WHAT IS CLAIMED IS:

1. A method of transferring data from circuitry disposed in a lower frequency clock domain to circuitry disposed in a higher frequency clock domain, said lower frequency clock domain operating with a first clock signal and said higher frequency clock domain operating with a second clock signal, comprising the steps:

latching said data in a latch gated by said first clock signal to generate latched data;

providing said latched data to a first register in said higher frequency clock domain to generate registered data, said first register operating responsive to a modified clock signal synthesized at least in part from said second clock signal; and

providing said registered data to a second register in said higher frequency clock domain to generate a synchronized data output, said second register operating responsive to said second clock signal.

2. The method of transferring data as set forth in claim 1, wherein said first and second clock signals are provided at a ratio of [M:N], where N equals the number of cycles of said second clock signal and M equals the number of cycles of said first clock signal and further equals (N-1), said cycles of said first and second clock signals being disposed between two substantially coincident rising edges of said first and second clocks signals that demarcate a coincident edge (CE) interval.

3. The method of transferring data as set forth in claim 2, wherein said modified clock signal is manufactured by a logic circuit based on a plurality of intermediary clock signals that are generated based on said second clock signal, and further wherein said intermediary clock signals comprise CHOP_CORE1, CHOP_CORE2, CHOP_CORE3 and CHOP_CORE4 signals, each of which signals is derived in a particular relationship with respect to said second clock signal.

4. The method of transferring data as set forth in claim 3, wherein said CHOP_CORE1 signal is generated such that its rising edge is triggered based on an (N-1)th rising edge of said second clock signal in a particular CE interval and its falling edge is triggered based on an (N-M)th rising edge of said second clock signal in a CE interval immediately following said particular CE interval.

5. The method of transferring data as set forth in claim 4, wherein said CHOP_CORE2 signal is generated such that its rising edge is triggered based on an (N-M)th falling edge of said second clock signal in said particular CE interval and its falling edge is triggered based on an (N-M)th rising edge of said second clock signal in a CE interval immediately following said particular CE interval.

6. The method of transferring data as set forth in claim 5, wherein said CHOP_CORE3 signal is generated such that its falling edge is triggered based on an (N-(M-1))th rising edge of said second clock signal in said particular CE interval and its rising edge is triggered based on an (N-(M-1))th falling edge of said second clock signal in said particular CE interval.

7. The method of transferring data as set forth in claim 6, wherein said CHOP_CORE4 signal is generated such that its falling edge is triggered based on an (N-1)th falling edge of said second clock signal in said particular CE interval and its rising edge is triggered based on an Nth rising edge of said second clock signal in said particular CE interval.

8. The method of transferring data as set forth in claim 7, wherein said rising edge of said CHOP_CORE1 signal is delayed by a propagation delay of approximately about 400 picoseconds from said (N-1)th rising edge of said second clock signal in said particular CE interval.

9. The method of transferring data as set forth in claim 8, wherein said falling edge of said CHOP_CORE1 signal is delayed by a propagation delay of approximately about 400 picoseconds from said (N-M)th rising edge of said second clock signal in said CE interval immediately following said particular CE interval.

10. The method of transferring data as set forth in claim 7, wherein said rising edge of said CHOP_CORE2 signal is delayed by a propagation delay of approximately about 400 picoseconds from said (N-M)th falling edge of said second clock signal in said particular CE interval.

11. The method of transferring data as set forth in claim 10, wherein said falling edge of said CHOP_CORE2 signal is delayed by a propagation delay of approximately about 400 picoseconds from said (N-M)th rising edge of said second clock signal in said CE interval immediately following said particular CE interval.

12. The method of transferring data as set forth in claim 7, wherein said falling edge of said CHOP_CORE3 signal is delayed by a propagation delay of approximately about 1200 picoseconds from said (N-(M-1))th rising edge of said second clock signal in said particular CE interval.

13. The method of transferring data as set forth in claim 12, wherein said rising edge of said CHOP_CORE3 signal is delayed by a propagation delay of approximately about 1200 picoseconds from said (N-(M-1))th falling edge of said second clock signal in said particular CE interval.

14. The method of transferring data as set forth in claim 7, wherein said falling edge of said CHOP_CORE4 signal is delayed by a propagation delay of approximately about 800 picoseconds from said (N-1)th falling edge of said second clock signal in said particular CE interval.

15. The method of transferring data as set forth in claim 14, wherein said rising edge of said CHOP_CORE4 signal is delayed by a propagation delay of approximately about 800 picoseconds from said Nth rising edge of said second clock signal in said particular CE interval.

16. The method of transferring data as set forth in claim 7, wherein said logic circuit is comprised of an OR gate for ORing said CHOP_CORE1 and second clock signals and an AND gate operable to accept said CHOP_CORE2, CHOP_CORE3 and CHOP_CORE4 signals for ANDing with an output generated by said OR gate.

17. A method of transferring data across a clock domain boundary, comprising the steps:

latching data provided by circuitry disposed in a first frequency domain to generate latched data, said latching step being gated in conjunction with a first clock signal actuating said first frequency domain;

providing said latched data to a first register clocked by a modified clock signal that is synthesized based on a second clock signal and four intermediary clock signals derived from said second clock signal, said first register operating to output registered data;

providing said registered data to a second register clocked by said second clock signal, said second register operating to generate a data output synchronized to said second clock signal; and

providing said data output to circuitry disposed in a second frequency domain actuated by said second clock signal,

wherein said first clock signal operates at a lower frequency and said second clock signal operates at a higher frequency, said lower and higher frequencies being related in a ratio of [M:N], where N equals the number of cycles of said second clock signal and M equals the number of cycles of said first clock signal and further equals (N-1), said cycles of said first and second clock signals being disposed between two substantially coincident rising edges of said first and second clocks signals that demarcate a coincident edge (CE) interval.

18. The method of transferring data across a clock domain boundary as set forth in claim 17, wherein first frequency domain is a bus clock domain in a computer system.

19. The method of transferring data across a clock domain boundary as set forth in claim 18, wherein second frequency domain is a core clock domain in a computer system.

20. The method of transferring data across a clock domain boundary as set forth in claim 17, wherein a first intermediary clock signal is generated such that its rising edge is triggered with a propagation delay of about 400 picoseconds from an (N-1)th rising edge of said second clock signal in a particular CE interval and its falling edge is triggered with a propagation delay of 400 picoseconds from an (N-M)th rising edge of said second clock signal in a CE interval immediately following said particular CE interval.

21. The method of transferring data across a clock domain boundary as set forth in claim 17, wherein a second intermediary clock signal is generated such that its rising edge is triggered with a propagation delay of about 400 picoseconds from an (N-M)th falling edge of said second clock signal in a particular CE interval and its falling edge is triggered with a propagation delay of about 400 picoseconds from an (N-M)th rising edge of said second clock signal in a CE interval immediately following said particular CE interval.

22. The method of transferring data across a clock domain boundary as set forth in claim 17, wherein a third intermediary clock signal is generated such that its falling edge is triggered with a propagation delay of about 1200 picoseconds from an (N-(M-1))th rising edge of said second clock signal in a particular CE interval and its rising edge is triggered with a propagation delay of about 1200 picoseconds from an (N-(M-1))th falling edge of said second clock signal in said particular CE interval.

23. The method of transferring data across a clock domain boundary as set forth in claim 17, wherein a fourth intermediary clock signal is generated such that its falling edge is triggered with a propagation delay of about 800 picoseconds from a (N-1)th falling edge of said second clock signal in a particular CE interval and its rising edge is triggered with a propagation delay of about 800 picoseconds from an Nth rising edge of said second clock signal in said particular CE interval.

24. A system for transferring data from circuitry disposed in a first clock domain to circuitry disposed in a second clock domain, said first clock domain operating with a first clock signal and said second clock domain operating with a second clock signal, comprising:

a latch gated by said first clock signal operable to generate latched data based on data from said circuitry disposed in said first clock domain;

a first register disposed in said second clock domain operable to generate registered data upon receiving said latched data from said latch, said first register operating responsive to a modified clock signal synthesized at least in part from said second clock signal;

a logic circuit operable to generate said modified clock signal based on said second clock signal and a plurality of intermediary clock signals derived from said second clock signal; and

a second register in said second clock domain to generate a synchronized data output upon receiving said registered data, said second register operating responsive to said second clock signal to provide said synchronized data output to said circuitry disposed in said second clock domain.

25. The system for transferring data as set forth in claim 24, wherein said first and second clock signals are provided at a ratio of [M:N], where N equals the number of cycles of said second clock signal and M equals the number of cycles of said first clock signal and further equals (N-1), said cycles of said first and second clock signals being disposed between two substantially coincident rising edges of said first and second clocks signals that demarcate a coincident edge (CE) interval.

26. The system for transferring data as set forth in claim 25, wherein said intermediary clock signals comprise CHOP_CORE1, CHOP_CORE2, CHOP_CORE3 and CHOP_CORE4 signals, each of which signals is derived in a particular relationship with respect to said second clock signal.

27. The system for transferring data as set forth in claim 26, wherein said logic circuit is comprised of an OR gate for ORing said CHOP_CORE1 and second clock signals and an AND gate operable to accept said CHOP_CORE2, CHOP_CORE3, CHOP_CORE4 signals for ANDing with an output generated by said OR gate.

28. The system for transferring data as set forth in claim 26, wherein said CHOP_CORE1 signal is generated such that its rising edge is triggered with a propagation delay of about 400 picoseconds from an (N-1)th rising edge of said second clock signal in a particular CE interval and its falling edge is triggered with a propagation delay of about 400 picoseconds from an (N-M)th rising edge of said second clock signal in a CE interval immediately following said particular CE interval.

29. The system for transferring data as set forth in claim 26, wherein said CHOP_CORE2 clock signal is generated such that its rising edge is triggered with a propagation delay of about 400 picoseconds from an (N-M)th falling edge of said second clock signal in a particular CE interval and its falling edge is triggered with a propagation delay of about 400 picoseconds from an (N-M)th rising edge of said second clock signal in a CE interval immediately following said particular CE interval.

30. The system for transferring data as set forth in claim 26, wherein said CHOP_CORE3 signal is generated such that its falling edge is triggered with a propagation delay of about 1200 picoseconds from an (N-(M-1))th rising edge of said second clock signal in a particular CE interval and its rising edge is triggered with a propagation delay of about 1200 picoseconds from an (N-(M-1))th falling edge of said second clock signal in said particular CE interval.

31. The system for transferring data as set forth in claim 26, wherein said CHOP_CORE4 signal is generated such that its falling edge is triggered with a propagation delay of about 800 picoseconds from an (N-1)th falling edge of said second clock signal in a particular CE interval and its rising edge is triggered with a propagation delay of about 800 picoseconds from an Nth rising edge of said second clock signal in said particular CE interval.

32. The system for transferring data as set forth in claim 24, wherein said first and second clocks are provided at a ratio of [1:1], and further wherein said intermediary clock signals comprise CHOP_CORE1, CHOP_CORE2, CHOP_CORE3 and CHOP_CORE4 signals such that CHOP_CORE1 = 0 and CHOP_CORE2 = CHOP_CORE3 = CHOP_CORE4 = 1.